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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/707,521	11/06/2000	Amelia C. Luna	SONY-50P3845	9729

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EXAMINER	
REKSTAD, ERICK J	

ART UNIT	PAPER NUMBER
2613	8

DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/707,521	Applicant(s) LUNA ET AL.	
	Examiner Erick Rekstad	Art Unit 2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a final rejection for application no. 09/707,521 in response to amendment filed on April 5, 2004.

Response to Arguments

In regards to applicants' arguments against the rejection of claims 1, 2, 3, 6, 10, 11, 12, 15, 18, 19, 20 and 22 under 35 U.S.C. 102(e) as being anticipated by US Patent 6,172, 621 to Iwata. The applicants argue that Iwata teaches only a sequential decoding process where the preparsing is preformed then the variable length decoding is performed. The applicants argue that the claimed invention has the preparsing and variable length decoding performed at the same time. Iwata teaches the method/system for decoding video using parallel processing (Col 11 Line 17-Col 13 Line 36, Fig. 8, 13-16). Note that Figure 16 shows the invention of Iwata performing multiple functions at the same time. Iwata further teaches the known decoding process where each function is performed on separate processors (Fig. 5), specifically preparsing function (91) and variable length decoding function (92). Iwata teaches that the processors of the invention use programs stored in memory to perform the desired functions (Col 11 Lines 24-29). Iwata further states that the invention has been described by reference to specific embodiments but numerous modifications could be made thereto by those skilled in the art without departing from the basic concept and scope of the invention (Col 18 Lines 15-20). Iwata does not specifically teach the preparsing and variable length decoding being performed in separate processors and

running in parallel. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Iwata with the known prior art decoding system in order to perform each function on a separate processor.

Applicant's arguments with respect to claims 4, 5, 7-9, 13, 14, 16, 17, 21, 23-29, and 30-37 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 3, 6, 10, 11, 12, 15, 18, 19, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,172,621 to Iwata.

[claims 1, 6, 10, 15, 18, 20, and 22]

Iwata teaches the method, computer-readable medium, and apparatus for decoding video using parallel processing involving the steps of preparsing, variable length decoding, decompressing, and de-shuffling (Col 11 Line 17-Col 13 Line 36, Fig. 8, 13-16). Note that Figure 16 shows the invention of Iwata performing multiple functions at the same time. Iwata further teaches the known decoding process where each function is performed on separate processors (Fig. 5), specifically preparsing function (91) and variable length decoding function (92). Iwata teaches that the

processors of the invention use programs stored in memory to perform the desired functions (Col 11 Lines 24-29). Iwata further states that the invention has been described by reference to specific embodiments but numerous modifications could be made thereto by those skilled in the art without departing from the basic concept and scope of the invention (Col 18 Lines 15-20). Iwata does not specifically teach the preparsing and variable length decoding being performed in separate processors and running in parallel. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Iwata with the known prior art decoding system in order to perform each function on separate processor in parallel (Official Notice).

[claims 2, 3, 11, 12, 19]

The digital video data is processed as a continues pipeline. While one unit is processing a first plurality of said digital video data a second unit is processing a second plurality of said digital video data (Col 4 Lines 7-12).

Claims 7, 8, 9, 16, 17, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata in view of US Patent 6,389,171 to Washington.

[claims 7, 8, 9,16,17, 28 and 29]

Iwata teaches the use of a digital video data decoder (Col 1 Lines 7-13, Fig. 5-6). Iwata does not specifically teach that the digital video data is mpeg or DV. Iwata also does not teach the use of Huffman code format for the encoded digital video data. Washington teaches that mpeg and DV are well know digital data formats that use Huffman coding to encode digital data in an ever smaller space in efforts to make digital

cameras and digital camcorders more attractive for the users (Col 1 Lines 32-38, Lines 57-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the digital video data formats mpeg or DV, which both use Huffman encoding, with Iwata's decoder in order to provide a decoder for the increasingly popular encoding techniques used in digital camcorders, as taught by Washington.

Claims 21, 23, 24, 25, 26, 30, 31, 32, 33, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata in view of US Patent 5,363,097 to Jan. [claims 21, 23, 24, 25, 26, 30, 31, 32, 33, and 34]

Iwata teaches the use of a digital video decoder containing a preparser, vld, and a de-shuffler as shown above for the rejection of claim 20. Iwata does not teach the use of a two way buffering between each stage of the decoding process. Jan teaches the use of a controlled data buffer for reading and writing data between the different stages of the decoding process in order to satisfy a system data rate (Col 5 Lines 58-68, Col 6 Lines 1-10, Fig. 3-5). Though Jan does not specifically say that the buffer controller is DMA, DMA is well know in the art (Official Notice). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Iwata's video decoder with the buffer system of Jan in order to satisfy a system's data rate requirements.

Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata and Jan as applied to claim 30 above, and further in view of Washington. [claims 36 and 37]

Iwata and Jan teach the use of a digital video data decoder comprising a first memory buffer, a processor, a variable length decoding unit (VLD), and a second

memory buffer. Iwata and Jan do not teach the use of the digital data in the DV format. Iwata does not teach the use of Huffman code format. Jan teaches the use of Huffman coding in a VLD in order to generate a fixed-length code word (Col 5 Lines 46-51). Washington teaches that mpeg and DV are well know digital data formats that use Huffman coding to encode digital data in an ever smaller space in efforts to make digital cameras and digital camcorders more attractive for the users (Col 1 Lines 32-38, Lines 57-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the digital video data formats mpeg or DV, which both use Huffman encoding, with the decoder of Iwata and Jan in order to provide a decoder for the increasingly popular encoding techniques used in digital camcorders, as taught by Washington.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata and Jan as applied to claim 30 above, and further in view of US Patent 6,496,199 to Peng et al.

[claim 30]

Iwata and Jan teach the use of a digital video decoder containing a preparser, vld, and a de-shuffler as shown above for claim 30. Iwata and Jan do not teach the use of a Very Long Instruction Word (VLIW) processor. Peng teaches the use of a VLIW CPU to control a system-on-a-chip video decoder in order to implement an advanced multimedia system at an affordable cost and with a smaller footprint (Col 1 Lines 50-55, Lines 59-63). The VLIW CPU contains an on-chip instruction cache that could obviously be used to store instructions on preparsing video data. The steps of the

decoder are obviously controlled under time sharing criteria because a real-time digital video decoder is required to perform the decoding steps in a specific amount of time. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the decoding method of Iwata and Jan with the system of Peng in order to produce an affordable and small advanced multimedia system.

Claims 4, 5, 13, 14, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata in view of US Patent 6,496,199 to Peng et al.

[claims 4, 5, 13, 14, and 27]

Iwata teaches the use of a digital video decoder containing a preparser, vld, and a de-shuffler as shown above for claims 1, 10 and 18. Iwata does not teach the use of a Very Long Instruction Word (VLIW) processor. Peng teaches the use of a VLIW CPU to control a system-on-a-chip video decoder in order to implement an advanced multimedia system at an affordable cost and with a smaller footprint (Col 1 Lines 50-55, Lines 59-63). The VLIW CPU contains an on-chip instruction cache that could obviously be used to store instructions on preparsing video data. The steps of the decoder are obviously controlled under time sharing criteria because a real-time digital video decoder is required to perform the decoding steps in a specific amount of time. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the decoding method of Iwata with the system of Peng in order to produce an affordable and small advanced multimedia system.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erick Rekstad whose telephone number is 703-305-5543. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 703-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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